SIGNETICS INTEGRATED CIRCUITS

TTL II 54H00 and 74H00 Series

Rating	Value	Unit
Supply Voltage - V_{CC}	+7.0	V
Input Voltage - V_{in}	+5.5	V
Output Voltage - V_{out}	+5.5	V
Operating Temperature Range	-55 to +125	°C

Function	Type/Pkg	Fan-Out	Supply Voltage
Quad 2-Input Positive NAND Gate	54H00/C,D	10	5
Quad 2-Input Positive NAND Gate (O.C.)	54H01/C,D	10	5
Quad 2-Input Positive AND Gate	54H08/C,D	10	5
Triple 3-Input Positive NAND Gate	54H10/C,D	10	5
Triple 3-Input Positive AND Gate	54H11/C,D	10	5
Dual 4-Input Positive NAND Gate	54H20/C,D	10	5
Dual 4-Input AND Gate	54H21/C,D	10	5
Dual 4-Input NAND Gate (O.C.)	54H22/C,D	10	5
8-Input Positive NAND Gate	54H30/C,D	10	5
Dual 4-Input Positive NAND Buffer	54H40/C,D	30	5
4-Wide 2-2-2-3 Input AND-OR-INVERT Gate	54H52/C,D	10	5
Expandable 2-2-2-3 Input AND-OR-INVERT Gate	54H53/C,D	10	5
Expandable 2-2-2-3 Input AND-OR-INVERT Gate	54H54/C,D	10	5
Expandable 2-Wide 4-Input AND-OR-INVERT Gate	54H55/C,D	10	5
Dual 4-Input Expander	54H60/C,D	—	4.5-5.5
Triple 3-Input Expander for AND-OR Gates	54H61/C,D	—	5
4-Wide 3-2-2-3 Input Expander for AOI Gates	54H62/C,D	—	4.5-5.5
J-K Master-Slave Flip-Flop	54H71/C,D	10	5
J-K Master-Slave Flip-Flop	54H72/C,D	10	5

Dual J-K Master-Slave Flip-Flop	54H73/C,D	10	5
Dual Type D Edge-Triggered Flip-Flop	54H74/C,D	10 - 20	5
Dual J-K Master-Slave Flip-Flop	54H76/E,F	10	5
J-K Edge-Triggered Flip-Flop	54H101/C,D	10	5
J-K Edge-Triggered Flip-Flop with AND Inputs	54H102/C,D	10	5
Dual J-K Edge-Triggered Flip-Flop	54H103/C,D	10	5
Dual J-K Edge-Triggered Flip-Flop	54H106/E,F	10	5
Dual J-K Edge-Triggered Flip-Flop	54H108/C,D	10	5